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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Su, *et al.* Docket No.: TSM03-0150  
Filed: September 30, 2003 Examiner: Fernando L. Toledo  
Serial No.: 10/675,862 Art Unit: 2823  
Title: Apparatus And Method For Manufacturing A Semiconductor Wafer With Reduced Delamination And Peeling

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Dear Sir:

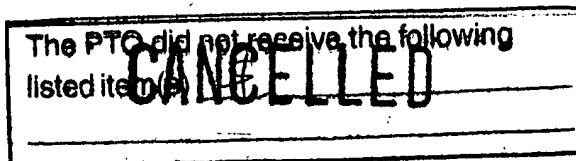
Applicant wishes to bring to the attention of the U.S. Patent and Trademark Office the information noted on the enclosed PTO Form PTO/SB/08A, which may be considered material to the examination of the above-identified application. Copies of the U.S. Patents cited are not being submitted. However, Applicant has included a copy of the non-patent literature.

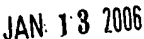
This Information Disclosure Statement is submitted under 37 C.F.R. §1.97(c) together with a \$180.00 fee under 37 C.F.R. §1.17(p) after the C.F.R. §1.97(b) time period, but before final action or notice of allowance, whichever occurs first.

Respectfully submitted,

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**Complete if Known**

Application Number	10/675,862
Filing Date	September 30, 2003
First Named Inventor	Su, <i>et al.</i>
Art Unit	2823
Examiner Name	Fernando L. Toledo
Attorney Docket Number	TSM03-0150

Sheet	1	of	1
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## U.S. PATENT DOCUMENTS

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	3	PIDIN, S., <i>et al.</i> , "MOSFET Current Drive Optimization Using Silicon Nitride Capping Layer for 65-nm Technology Node," 2004 Symposium on VLSI Technology Digest of Technical Papers, pp. 54-55.	

Examiner Signature		Date Considered	
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Date of Deposit: January 10, 2006

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Information Disclosure Statement (1 original and 1 copy)  
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Respectfully submitted,

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